

## WEST Search History

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DATE: Wednesday, November 24, 2004

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>			
<input type="checkbox"/>	L83	(cpu or processor) with L82	3
<input type="checkbox"/>	L82	l14 with (fpga or pld)	52
<input type="checkbox"/>	L81	cpu with L79	12
<input type="checkbox"/>	L80	processor with L79	29
<input type="checkbox"/>	L79	l14 with (programmable gate\$1 or programmable logic)	184
<input type="checkbox"/>	L78	L77 not (l65 or l63 or l61 or l60 or l58 or l70 or l75)	220
<input type="checkbox"/>	L77	processor with l74	265
<input type="checkbox"/>	L76	L75 not (l65 or l63 or l61 or l60 or l58 or l70)	2
<input type="checkbox"/>	L75	cpu same L74	36
<input type="checkbox"/>	L74	l15 with (programmable gate\$1 or programmable logic)	1202
<input type="checkbox"/>	L73	L70 not (l65 or l63 or l61 or l60 or l58)	14
<input type="checkbox"/>	L72	L70 not l58	14
<input type="checkbox"/>	L71	L70 not l60	16
<input type="checkbox"/>	L70	cpu same L69	22
<input type="checkbox"/>	L69	l15 with (fpga or pld)	572
<input type="checkbox"/>	L68	l15 same (fpga or pld)	1225
<i>DB=USPT,USOC; PLUR=NO; OP=ADJ</i>			
<input type="checkbox"/>	L67	L66 not (l65 or l63 or l61 or l60 or l58)	37
<input type="checkbox"/>	L66	processor with l59	80
<input type="checkbox"/>	L65	processor with l62	42
<input type="checkbox"/>	L64	processor same l62	67
<input type="checkbox"/>	L63	core same L62	14
<input type="checkbox"/>	L62	l15 with (fpga or pld)	141
<input type="checkbox"/>	L61	L60 not l58	17
<input type="checkbox"/>	L60	cpu same L59	23
<input type="checkbox"/>	L59	l15 with (programmable gate\$1 or programmable logic)	413
<input type="checkbox"/>	L58	cpu same L57	16
<input type="checkbox"/>	L57	l15 same (fpga or pld)	327
<input type="checkbox"/>	L56	cpu and L55	356
<input type="checkbox"/>	L55	l15 and (fpga or pld)	985

<input type="checkbox"/>	L54	logic integrated circuit\$1 and l22	0
<input type="checkbox"/>	L53	l22 and (programmable gate\$1 or programmable logic)	0
<input type="checkbox"/>	L52	l22 and (fpga or pld)	0
<input type="checkbox"/>	L51	enabl\$3 and (L2 or L6)	2
<input type="checkbox"/>	L50	enabl\$3 and L49	1
<input type="checkbox"/>	L49	(L2 or L6) and programmable	1
<input type="checkbox"/>	L48	(L2 or L6) and logic	2
<input type="checkbox"/>	L47	L2 or L6 and logic	2
<input type="checkbox"/>	L46	cpu with L44	4
<input type="checkbox"/>	L45	reprogram\$4 with L44	4
<input type="checkbox"/>	L44	fpga with (simulat\$3 or emulat\$3)	299
		<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L43	reprogram\$4 with L42	0
<input type="checkbox"/>	L42	fpga with (simulat\$3 or emulat\$3)	79
<input type="checkbox"/>	L41	fpga simulator	0
		<i>DB=USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L40	US-6260172-B1.did.	1
<input type="checkbox"/>	L39	US-6089460-A.did.	1
<input type="checkbox"/>	L38	US-6260172-B1.did.	1
		<i>DB=PGPB; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L37	US-20010011214-A1.did.	1
<input type="checkbox"/>	L36	US-20010011214-A1.did.	1
		<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L35	cpu and L34	11
<input type="checkbox"/>	L34	logic integrated circuit\$1	904
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L33	5968161.uref.	6
<input type="checkbox"/>	L32	altera.as. and L31	1
<input type="checkbox"/>	L31	fpga same cpu	1147
<input type="checkbox"/>	L30	altera.as. and cpu	186
		<i>DB=USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L29	cpu and L27	35
<input type="checkbox"/>	L28	cpu core\$1 and L27	0
<input type="checkbox"/>	L27	L26 and L15	116
<input type="checkbox"/>	L26	L12.ti,ab,clm.	1427
<input type="checkbox"/>	L25	5933642.pn.	1
		<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L24	5933642.pn.	1

<input type="checkbox"/>	L23	L20 and L22	2
<input type="checkbox"/>	L22	firmware or nanoinstruction\$1 or nano-instruction\$1 or nanocode or nano-code or nanoprogram or nano-program or L21	15749
<input type="checkbox"/>	L21	microinstruction\$1 or micro-instruction\$1 or microcode or micro-code or micro-operation\$1 or microoperation\$1 or micro-op\$1 or microop\$1 or micro-program\$1 or microprogram\$1	11222
<input type="checkbox"/>	L20	cpu and L19	196
<input type="checkbox"/>	L19	field programmable gate array\$1 or fpga\$1	3251
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L18	cpu core\$1 and L17	12
<input type="checkbox"/>	L17	L12 same L15	1418
<input type="checkbox"/>	L16	L13 and L15	92
		<i>DB=USPT,PGPB; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L15	firmware or nanoinstruction\$1 or nano-instruction\$1 or nanocode or nano-code or nanoprogram or nano-program or L14	52363
<input type="checkbox"/>	L14	microinstruction\$1 or micro-instruction\$1 or microcode or micro-code or micro-operation\$1 or microoperation\$1 or micro-op\$1 or microop\$1 or micro-program\$1 or microprogram\$1	14283
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L13	cpu core\$1 and L12	135
<input type="checkbox"/>	L12	field programmable gate array\$1 or fpga\$1	16012
<input type="checkbox"/>	L11	L9 and core	2737
<input type="checkbox"/>	L10	(L2 or L6) and L9	0
<input type="checkbox"/>	L9	field programmable gate array\$1	12350
<input type="checkbox"/>	L8	(L2 or L6) and fpga	0
<input type="checkbox"/>	L7	(L2 or L6) and core	0
<input type="checkbox"/>	L6	5675777.pn.	1
<input type="checkbox"/>	L5	glickman.in. and jeff.in.	6
<input type="checkbox"/>	L4	glickman.in. and taraplex.as.	0
<input type="checkbox"/>	L3	glickman.in. and teraplex.as.	0
<input type="checkbox"/>	L2	6389528.pn.	1
<input type="checkbox"/>	L1	pappalardo.in. and tesi.in.	7

END OF SEARCH HISTORY